CLAIM AMENDMENTS

1. (Currently Amended) A semiconductor device comprising a driver circuit for ~~driving~~ supplying a voltage at an output node in accordance with an input signal received at an input node, ~~wherein~~ said driver circuit ~~includes~~ including:

a first transistor connected between a first voltage and said output node, and turned on and off in accordance with ~~a~~ voltage ~~level~~ of a first internal node;

a second transistor connected between said output node and a second voltage, and turned on and off complementarily to said first transistor, in accordance with ~~a~~ voltage of a second internal node; and

a control circuit controlling voltages of said first and second internal nodes ~~so as~~ to complementarily turn on said first and second transistors in accordance with ~~said~~ the input signal, said control circuit ~~has~~ including a voltage adjustment circuit connected to at least one of said first and second internal nodes, and, when the one of said first and second transistors corresponding to the internal node connected to said voltage adjustment circuit is turned on, in accordance with the voltage level of the ~~connected~~ internal node connected to said voltage adjustment circuit, said voltage adjustment circuit sets ~~the voltage of~~ said ~~connected~~ internal node connected to said voltage adjustment circuit at a voltage ~~level~~ different from the ~~voltage levels of said~~ first and second voltages.

2. (Currently Amended) The semiconductor device according to claim 1, wherein the voltage of said ~~connected~~ internal node connected to said voltage adjustment circuit is set ~~at~~ to one of ~~said~~ the first and second voltages when the corresponding transistor is turned on.

3. (Currently Amended) The semiconductor device according to claim 1, wherein

said control circuit ~~further has~~ includes a timing circuit ~~provided in correspondence with~~ corresponding to said at least one of said first and second internal nodes, and,

when the ~~corresponding~~ transistor corresponding to said internal node connected to said voltage adjustment circuit is turned on, said timing circuit connects one of ~~said~~ the first and second voltages ~~for turning on said corresponding transistor~~ to said ~~connected~~ internal node connected to said voltage adjustment circuit for a predetermined period.

4. (Currently Amended) The semiconductor device according to claim 3, wherein said timing circuit adjusts ~~said~~ the predetermined period in accordance with the voltage of said output node.

5. (Currently Amended) The semiconductor device according to claim 3, wherein

said timing circuit ~~has~~ includes a delay circuit for delaying ~~said~~ the input signal, and ~~said~~ the predetermined period corresponds to delay time ~~given by~~ of said delay circuit.

6. (Currently Amended) The semiconductor device according to claim 1, wherein

said control circuit sets the internal node of the other of said first and second transistors at one of ~~said~~ the first and second voltages for turning on ~~said corresponding~~ the transistor ~~so as~~ corresponding to that internal node and to turn off ~~said~~ the other ~~transistor when said corresponding transistor is turned on~~ of said first and second transistors, and

said control circuit further ~~has~~ includes a connection circuit ~~for~~ electrically connecting said first internal node ~~and~~ to said second internal node for a predetermined period when the ~~corresponding~~ transistor corresponding to said internal node is turned on.

7. (Currently Amended) The semiconductor device according to claim 6, wherein said connection circuit ~~has~~ includes a delay circuit delaying ~~said~~ the input signal, and ~~said~~ the predetermined period corresponds to delay time ~~given by~~ of said delay circuit.

8. (Currently Amended) The semiconductor device according to claim 1, wherein said first and second transistors are each ~~constituted by a~~ first and second field effect ~~transistor~~ transistors having ~~a~~ respective gate oxide ~~film~~ films, and said semiconductor device further comprises ~~another~~ a third field effect transistor having a ~~different~~ respective gate oxide film different from said gate oxide film of at least one of said first and second transistors.

9. (Currently Amended) The semiconductor device according to claim 1, wherein said first and second transistors are ~~each constituted by a~~ first and second field effect ~~transistor~~ transistors having ~~a~~ respective dielectric ~~film~~ films, and said semiconductor device further comprises ~~another~~ a third field effect transistor having a ~~different~~ dielectric film different from said dielectric film of ~~said~~ at least one of said first and second transistors.

10. (Currently Amended) The semiconductor device according to claim 1, wherein ~~said~~ the input signal includes a plurality of signals, and

said control circuit controls the voltages of said first and second internal nodes in accordance with a ~~predetermined~~ logic operation result based on ~~said~~ the plurality of signals.

11. (Currently Amended) The semiconductor device according to claim 10, wherein

said control circuit further ~~has~~ includes a timing circuit ~~provided on~~ connected to at least one of said first and second internal nodes, and

said timing circuit connects one of ~~said~~ the first and second voltages ~~for turning~~ on ~~said~~ a corresponding one of said first and second transistors transistor to said ~~connected~~ internal node connected to said voltage adjustment circuit for a predetermined period when ~~the corresponding~~ said transistor is turned on.

12. (Currently Amended) A semiconductor device comprising a driver circuit for ~~driving~~ supplying a voltage at an output node in accordance with an input signal received at an input node, ~~wherein~~ said driver circuit ~~includes~~ including:

a first transistor connected between a first voltage and said output node, and turned on and off in accordance with ~~a~~ voltage ~~level~~ of a first internal node;

a second transistor connected between said output node and a second voltage, and turned on and off in accordance with ~~a~~ voltage ~~level~~ of a second internal node;

a third transistor connected in parallel ~~to~~ with said second transistor, between said output node and ~~said~~ the second voltage, and turned on and off, complementarily to said first transistor, in accordance with the voltage ~~level~~ of said first internal node; and

a control circuit for controlling voltages of said first and second internal nodes ~~so as~~ to complementarily turn on said first transistor and said second and third transistors in accordance with ~~said~~ the input signal, said control circuit ~~sets~~ setting one of ~~said~~ the first and second voltages for turning on said second and third transistors to said first internal node ~~so as~~ and to turn off said first transistor when said second and third transistors are turned on, and ~~supplies said~~ supplying one of ~~said~~ the first and second voltages to said second internal node for a predetermined period, ~~and~~ wherein said second transistor has a driving force for supplying ~~said~~ the second voltage to said output node and higher than ~~that~~ a driving force of said third transistor.

13. (Currently Amended) The semiconductor device according to claim 12, wherein

said control circuit ~~has~~ includes a timing circuit ~~provided in correspondence with~~ corresponding to said second internal node, and

said timing circuit adjusts ~~said~~ the predetermined period in accordance with the voltage ~~level~~ of said output node.

14. (Currently Amended) The semiconductor device according to claim 12, wherein said control circuit ~~has~~ includes a connection circuit for electrically connecting said first internal node to said second internal node for ~~said~~ the predetermined period.

15. (Currently Amended) The semiconductor device according to claim 12, wherein ~~said~~ the input signal includes a plurality of signals, and

said control circuit controls the voltages of said first and second internal nodes in accordance with a result of a ~~predetermined~~ logic operation ~~performed~~ based on ~~said~~ the plurality of signals.

16. (Currently Amended) The semiconductor device according to claim 12, wherein

each of said first, second, and third transistors ~~is formed of a~~ are first, second and third field-effect ~~transistor~~ transistors having ~~a~~ respective gate oxide ~~film~~ films, and

said semiconductor device further comprises ~~another~~ a fourth field-effect transistor having a different gate oxide film from said gate oxide film of at least one of said first, second, and third transistors.

17. (Currently Amended) The semiconductor device according to claim 12, wherein said control circuit includes a noise adjustment circuit for supplying one of ~~said~~ the first and second voltages for turning on said second and third transistors to said first internal node in response to an external instruction in a standby state.

18. (Currently Amended) A semiconductor device comprising a first driver circuit and a second driver circuit ~~arranged to be~~ adjacent each other, each of the first and second driver circuits ~~driving~~ supplying a voltage at an output node in accordance with an input signal received at an input node, wherein each of said first and second driver circuits includes:

a first transistor connected between a first voltage and said output node, and turned on and off in accordance with a voltage ~~level~~ of a first internal node;

a second transistor connected between said output node and a second voltage, and turned on and off in accordance with a voltage ~~level~~ of a second internal node;

a third transistor connected in parallel ~~to~~ with said second transistor, between said output node and ~~said~~ the second voltage, and turned on and off, complementarily to said first transistor, in accordance with the voltage ~~level~~ of said first internal node; and

a control circuit for controlling voltages of said first and second internal nodes ~~so as~~ to complementarily turn on said first transistor and said second and third transistors in accordance with ~~said~~ the input signal, wherein

said control circuit of each of said first and second driver circuits sets one of ~~said~~ the first and second voltages for turning on said second and third transistors to said first internal node ~~so as~~ to turn off said first transistor when said second and third transistors are turned on, and supplies ~~said~~ the one of the first and second voltages to said second internal node for a predetermined period,

said second transistor has a driving force for supplying ~~said~~ the second voltage to said output node higher than ~~that~~ the driving force of said third transistor, and

said control circuit of each of said first and second driver circuits includes a noise adjustment circuit for supplying one of ~~said~~ the first and second voltages, for turning on said second and third transistors, to said second internal node, in accordance with the input signal ~~inputted~~ input to the ~~adjacent~~ other driver circuit in a standby state.